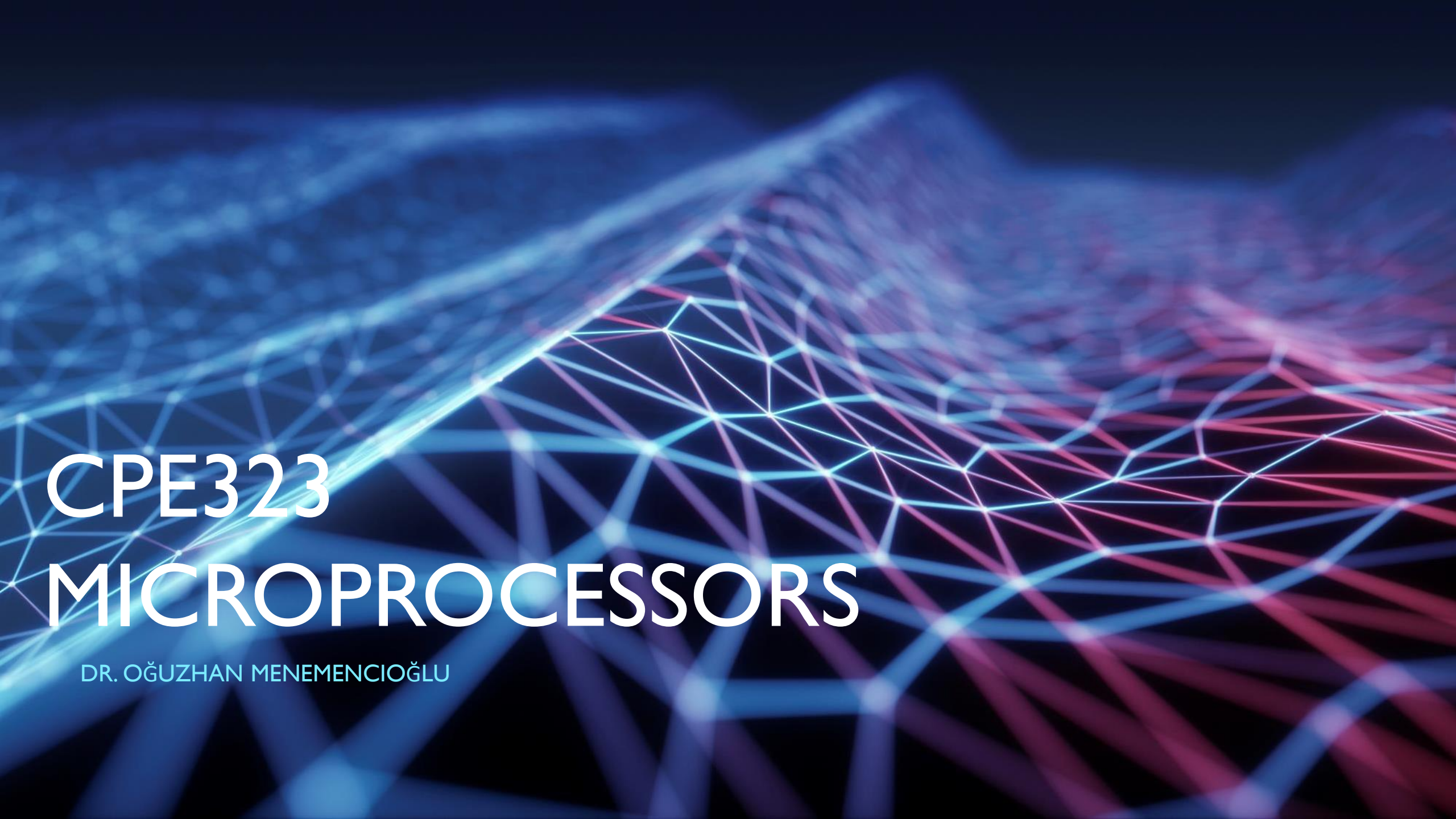


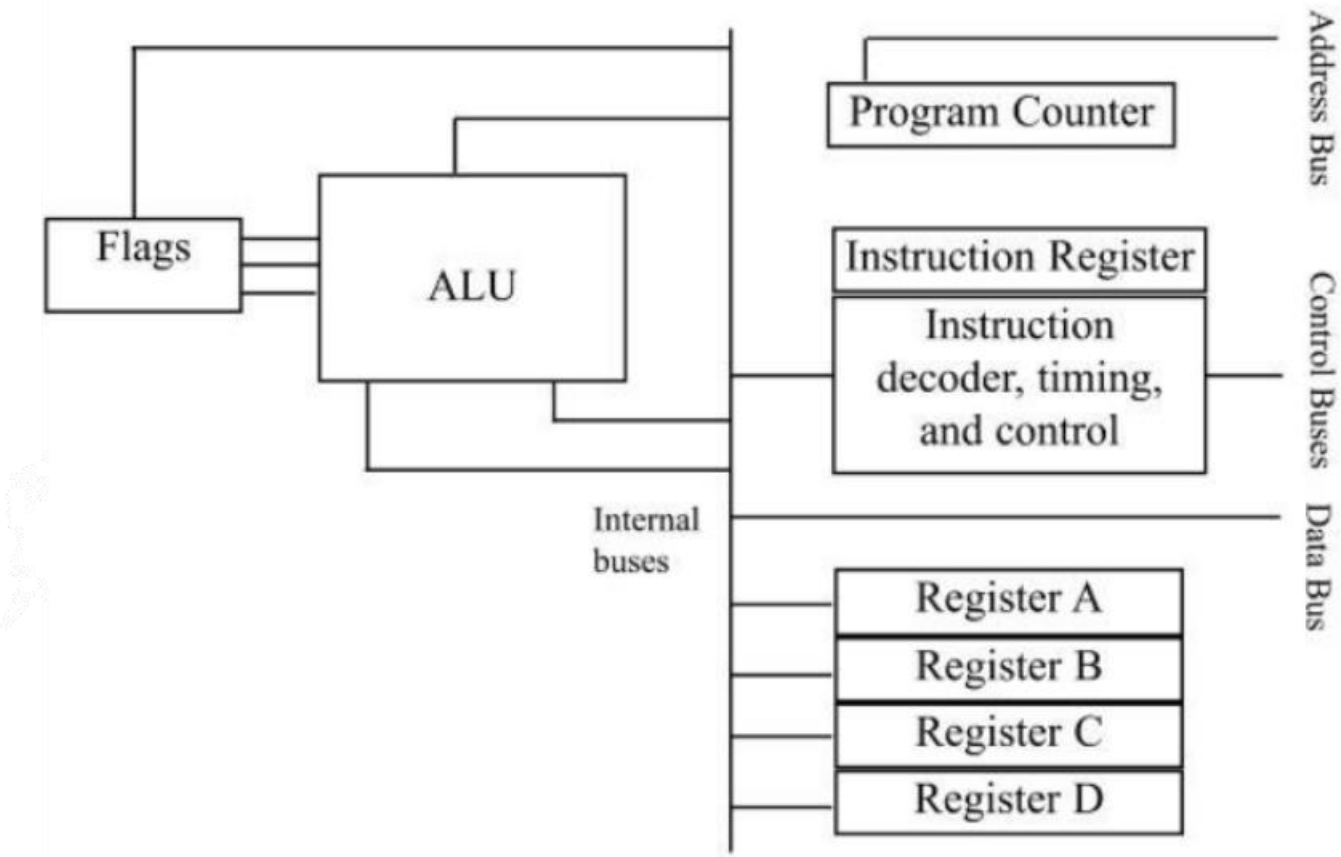
CPE323 MICROPROCESSORS

DR. OĞUZHAN MENEMENCIOĞLU

INTERNAL MICROPROCESSOR ARCHITECTURE

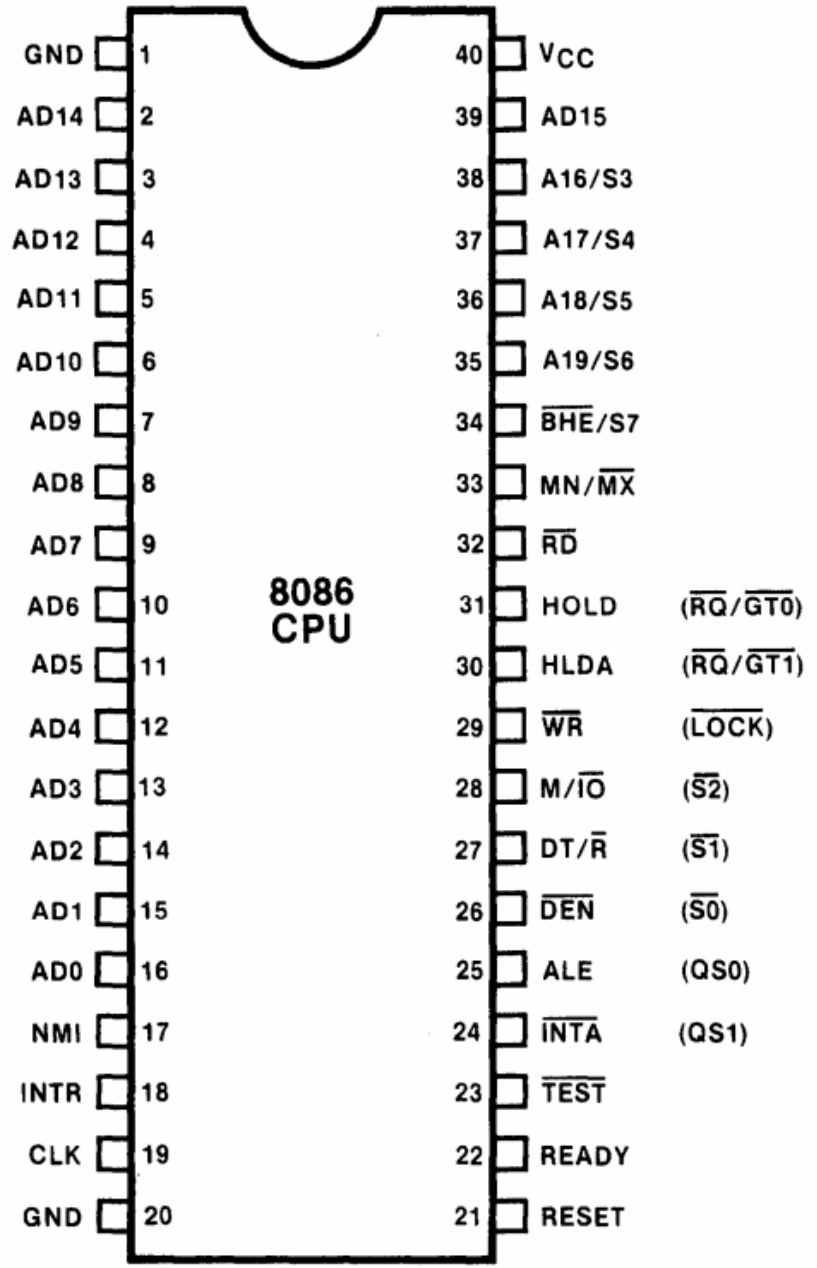
OUTLINE

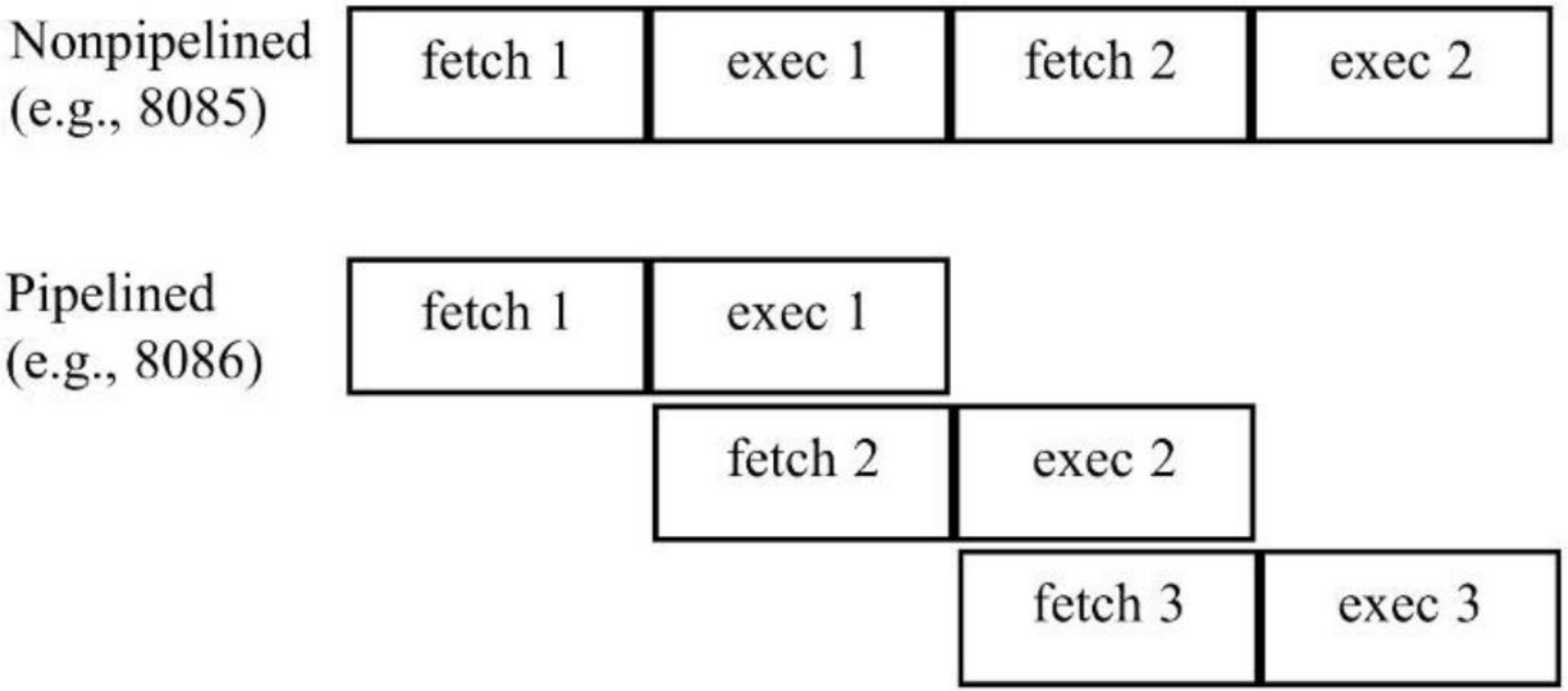
- Internal Microprocessor Architecture
  - Internal Block Diagram of CPU
  - Intel 8086 Pin Diagram
  - Internal block diagram of the 8086
  - The Programming Model
  - Multipurpose Registers
  - Special-Purpose Registers
  - List of Each Flag bit, with a brief description of function.
  - Segment Registers



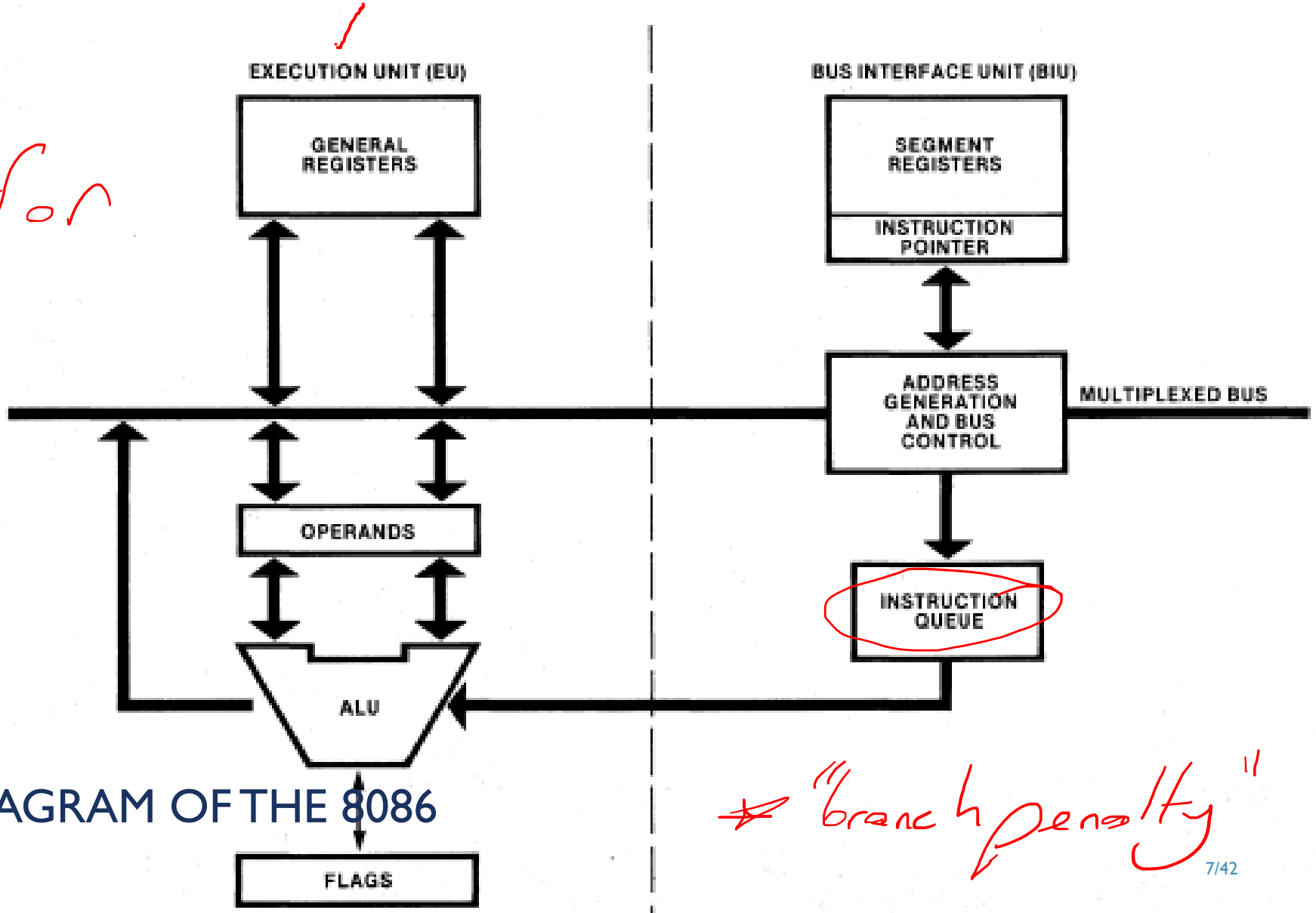
INTERNAL BLOCK DIAGRAM OF CPU

INTEL 8086 PIN DIAGRAM





PIPELINED VS. NONPIPELINED EXECUTION



INTERNAL BLOCK DIAGRAM OF THE 8086

INTERNAL MICROPROCESSOR ARCHITECTURE

- Before a program is written or instruction investigated, internal configuration of the microprocessor must be known.
- In a multiple core microprocessor each core contains the same programming model.
- Each core runs a separate task or thread simultaneously.

INTERNAL MICROPROCESSOR ARCHITECTURE

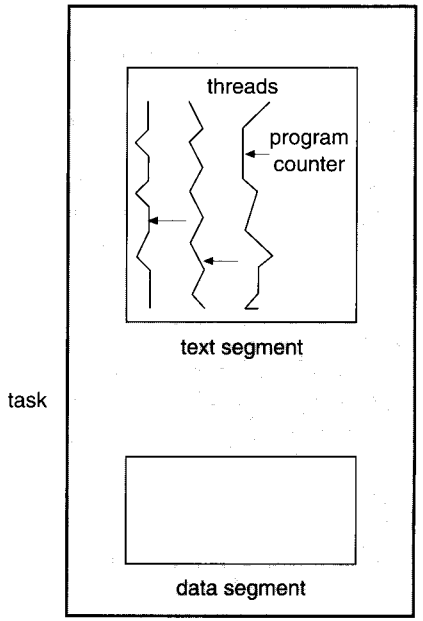


Figure 4.8 Multiple threads within a task.

- A thread consists of a program counter, a register set, and a stack space.
- A task shares with peer threads its code section, data section, and operating system resources

THE PROGRAMMING MODEL

- 8086 through Core2 considered **program visible**.
  - registers are used during programming and are specified by the instructions
- Other registers considered to be **program invisible**.
  - not addressable directly during applications programming

INTERNAL MICROPROCESSOR ARCHITECTURE

- 80286 and above contain program-invisible registers to control and operate protected memory.
  - and other features of the microprocessor
- 80386 through Core2 microprocessors contain full 32-bit internal architectures.
- 8086 through the 80286 are fully upward-compatible to the 80386 through Core2.
- Figure 2–1 illustrates the programming model 8086 through Core2 microprocessor.
  - including the 64-bit extensions

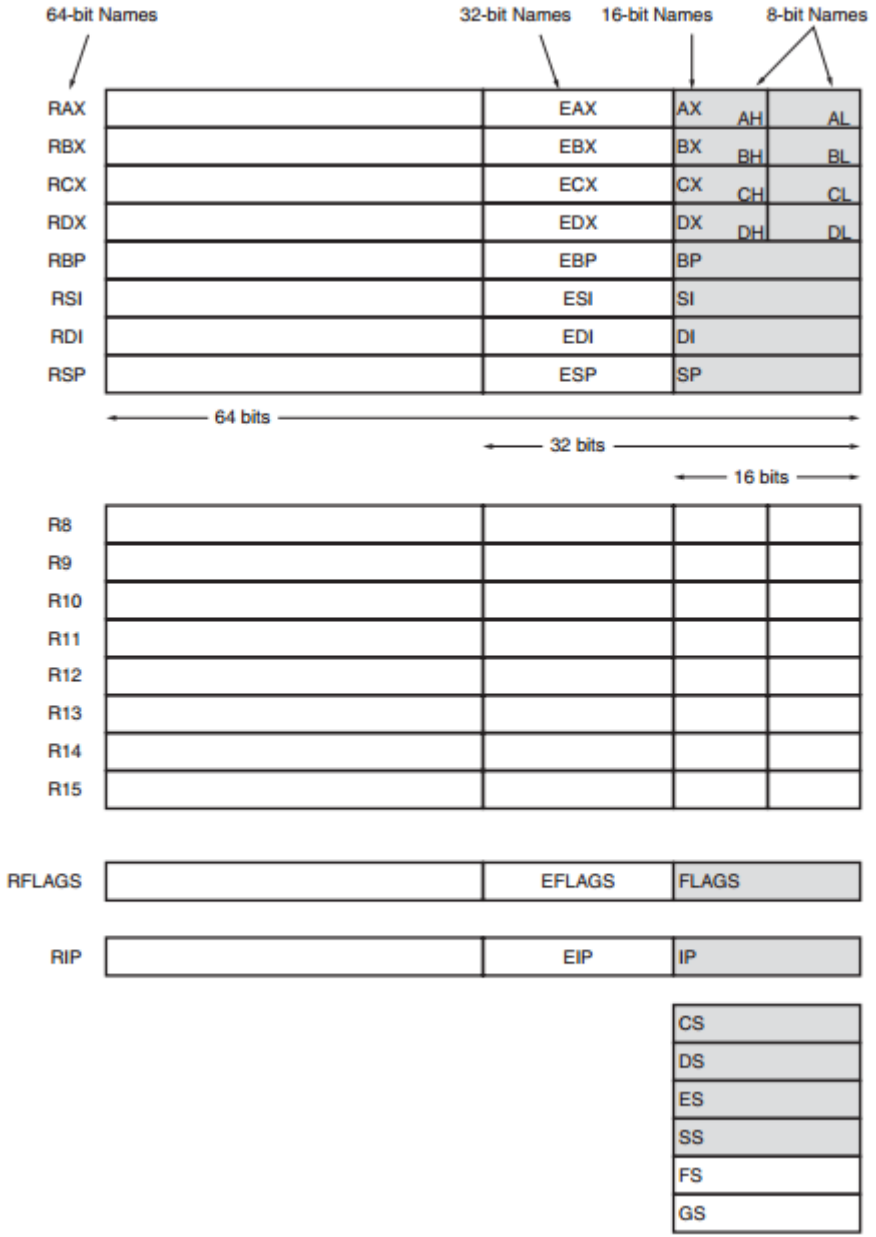


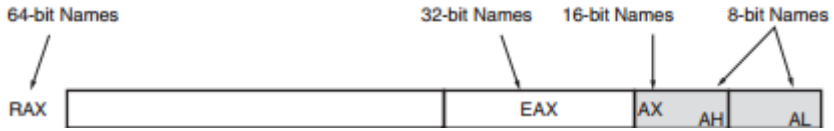
FIGURE 2–1 The programming model of the 8086 through the core2 microprocessor including the 64-bit extensions.

MULTIPURPOSE REGISTERS

- **RAX -** a 64-bit register (RAX), a 32-bit register **(accumulator)** (EAX), a 16-bit register (AX), or as either of two 8-bit registers (AH and AL).

- The accumulator is used for instructions such as multiplication, division, and some of the adjustment instructions.

- Intel plans to expand the address bus to 52 bits to address 4P (2^{52}~10^{15} =peta) bytes of memory.

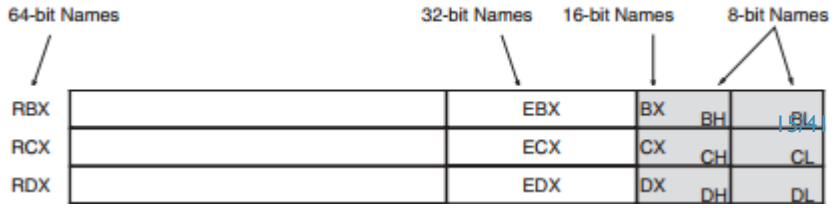


ADDRESS SPACE (MAIN MEMORY: RAM)

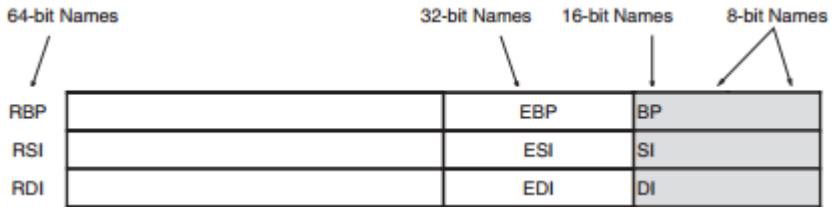
- Address bus:16 bit →Address Space:64 Kbytes (2^{16} = 65536 = 64 * 1024)
- Address bus:20 bit →Address Space:1 Mbytes (2^{20} = 1.048.576 = 1 * 1024 * 1024)
- Address bus:32 bit →Address Space:4 Gbytes (2^{32} = 4.294.967.296 = 4 * 1024 * 1024 * 1024)
- Address bus:34 bit →Address Space:16GBytes (2^{34} = 17.179.869.184 = 16 * 1024 * 1024 * 1024)
- Address bus:36 bit →Address Space:64GBytes (2^{36} = 68.719.476.736 = 64 * 1024 * 1024 * 1024)
- Address bus:38 bit →Address Space:256GBytes (2^{38} = 274.877.906.944 = 256 * 1024 * 1024 * 1024)
- Address bus:52 bit →Address Space:10^{15} Bytes (2^{52} = 4.503.599.627.370.496 ~ 10^{15} = 1.000.000.000.000.000)

MULTIPURPOSE REGISTERS

- **RBX,** addressable as RBX, EBX, BX, BH, BL.
  - BX register **(base index)** sometimes holds offset address of a location in the memory system in all versions of the microprocessor
- **RCX**, as RCX, ECX, CX, CH, or CL.
  - a **(count)** general-purpose register that also holds the count for various instructions
- **RDX,** as RDX, EDX, DX, DH, or DL.
  - a **(data)** general-purpose register
  - holds a part of the result from a multiplication or part of dividend before a division



MULTIPURPOSE REGISTERS



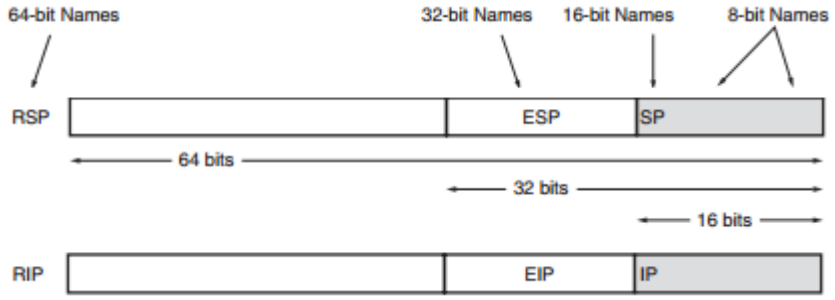
- **RBP,** as RBP, EBP, or BP.
  - points to a memory **(base pointer)** location for memory data transfers
- **RDI** addressable as RDI, EDI, or DI.
  - often addresses **(destination index)** string destination data for the string instructions
- **RSI** used as RSI, ESI, or SI.
  - the **(source index)** register addresses source string data for the string instructions
  - like RDI, RSI also functions as a general-purpose register

MULTIPURPOSE REGISTERS

- **R8 - R15** found in the Pentium 4 and Core2 if 64-bit extensions are enabled.
  - data are addressed as 64-, 32-, 16-, or 8-bit sizes and are of general purpose
- Most applications will not use these registers until 64-bit processors are common.
  - the 8-bit portion is the rightmost 8-bit only
  - bits 8 to 15 are not directly addressable as a byte

SPECIAL-PURPOSE REGISTERS

- Include RIP, RSP, and RFLAGS
  - segment registers include CS, DS, ES, SS, FS, and GS
- **RIP** addresses the next instruction in a section of memory.
  - defined as **(instruction pointer)** a code segment
- **RSP** addresses an area of memory called the stack.
  - the **(stack pointer)** stores data through this pointer

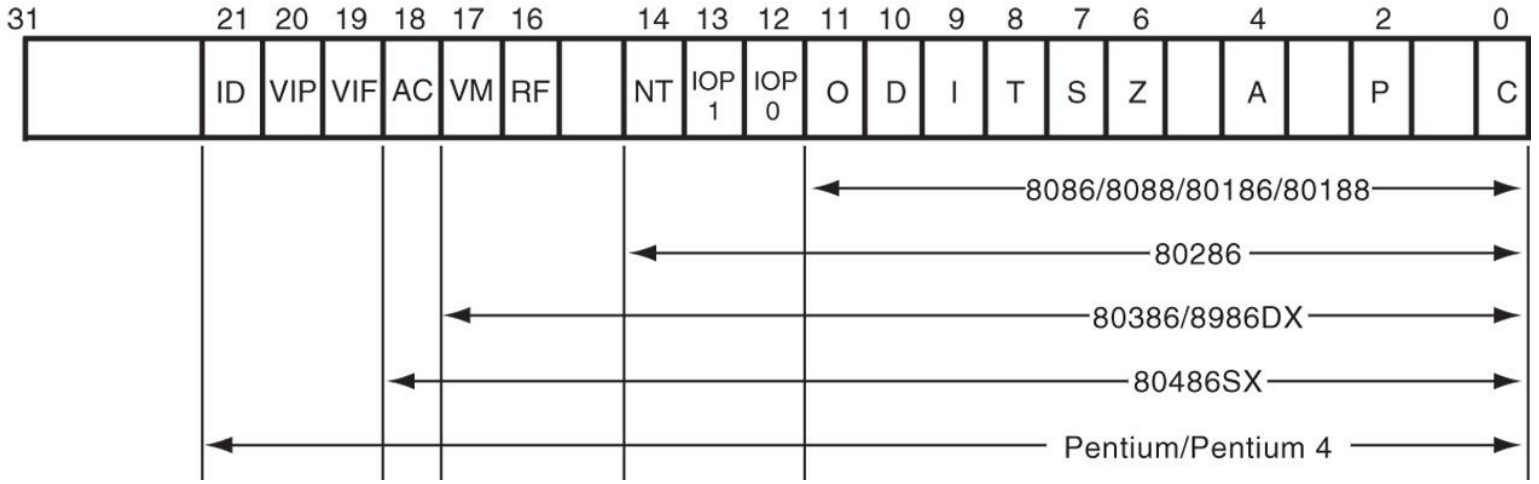


SPECIAL-PURPOSE REGISTERS

- **RFLAGS** indicate the condition of the microprocessor and control its operation.
- Figure 2–2 shows the flag registers of all versions of the microprocessor.
- Flags are upward-compatible from the 8086/8088 through Core2 .
- The rightmost five and the overflow flag are changed by most arithmetic and logic operations.
  - although data transfers do not affect them

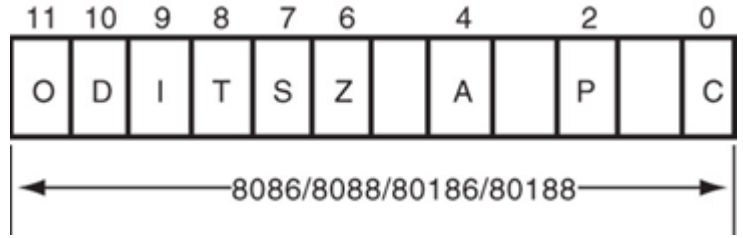
FIGURE 2–2 THE EFLAG AND FLAG REGISTER COUNTS FOR THE ENTIRE 8086 AND PENTIUM MICROPROCESSOR FAMILY.

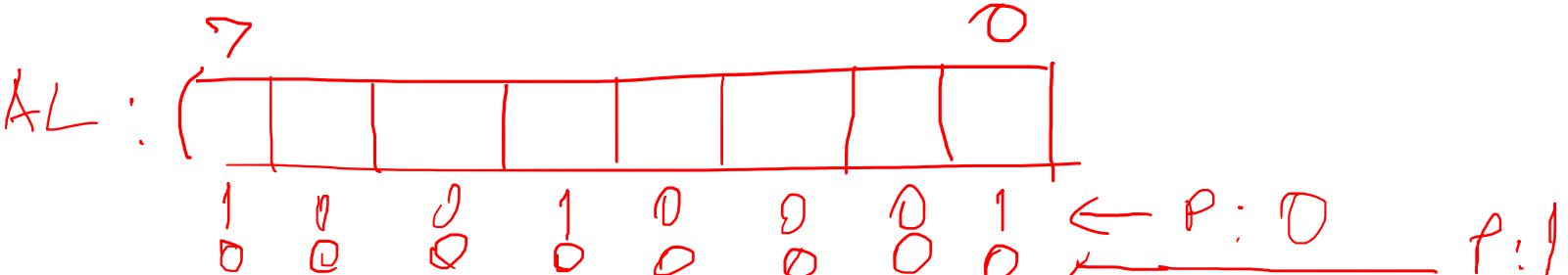
- Flags never change for any data transfer or program control operation.
- Some of the flags are also used to control features found in the microprocessor.



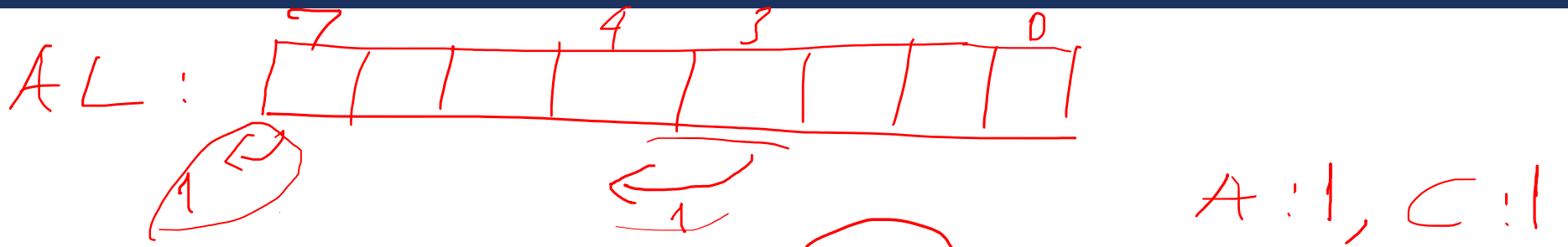
SPECIAL-PURPOSE REGISTERS

- Flag bits, with a brief description of function.
- **C (carry)** holds the carry after addition or borrow after subtraction.
  - also indicates error conditions
- **P (parity)** is the count of ones in a number expressed as even or odd. Logic 0 for odd parity; logic 1 for even parity.
  - if a number contains three binary one bits, it has odd parity
  - if a number contains no one bits, it has even parity

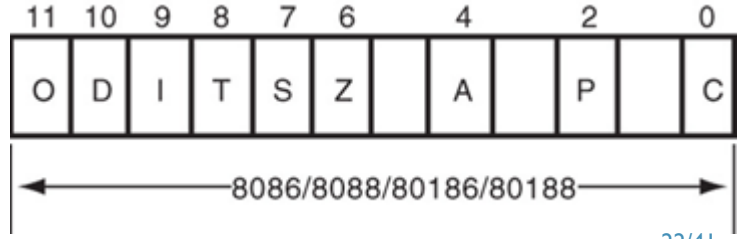




LIST OF EACH FLAG BIT, WITH A BRIEF DESCRIPTION OF FUNCTION.



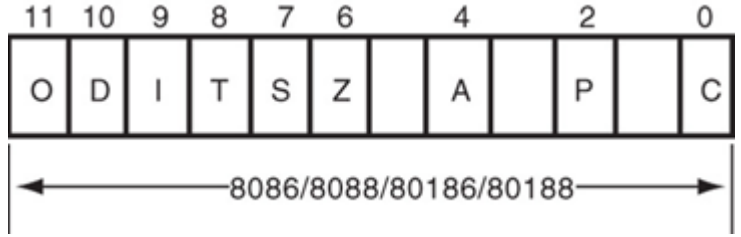
- **A (auxiliary carry)** holds the carry (half-carry) after addition or the borrow after subtraction between bit positions 3 and 4 of the result.
- **Z (zero)** shows that the result of an arithmetic or logic operation is zero.
- **S (sign)** flag holds the arithmetic sign of the result after an arithmetic or logic instruction executes.
- **T (trap)** The trap flag enables trapping through an on-chip debugging feature.



LIST OF EACH FLAG BIT, WITH A BRIEF DESCRIPTION OF FUNCTION.

- **I (interrupt)** controls operation of the INTR (interrupt request) input pin.
- **D (direction)** selects increment or decrement mode for the DI and/or SI registers.
- **O (overflow)** occurs when signed numbers are added or subtracted.
  - an overflow indicates the result has exceeded the capacity of the machine

8086 → 16

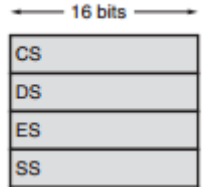


SEGMENT REGISTERS

- Generate memory addresses when combined with other registers in the microprocessor.
- Four or six segment registers in various versions of the microprocessor.
- A segment register functions differently in real mode than in protected mode.
- Following is a list of each segment register, along with its function in the system.

SEGMENT REGISTERS

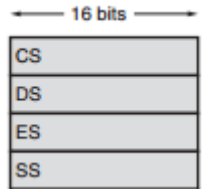
- **CS (code)** segment holds code (programs and procedures) used by the microprocessor.
- **DS (data)** contains most data used by a program.
  - Data are accessed by an offset address or contents of other registers that hold the offset address
- **ES (extra)** an additional data segment used by some instructions to hold destination data.



SEGMENT REGISTERS

- **SS (stack)** defines the area of memory used for the stack.
  - stack entry point is determined by the stack segment and stack pointer registers
  - the BP register also addresses data within the stack segment

coming soon ..



RESOURCES

- These slides are designed to accompany The Intel Microprocessors: 8086/8088, 80186/80188, 80286, 80386, 80486 Pentium, Pentium Pro Processor, Pentium II, Pentium, 4, and Core2 with 64-bit Extensions Architecture, Programming, and Interfacing, Pearson Education, Inc. , Eighth Edition. Slides copyright 2009 by Barry B. Brey.
- The 80x86 IBM PC and Compatible Computer, by M. A. Mazidi &. J. G. Mazidi, Prentice Hall, 4th Edition.

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